We claim:

1. A circuit arrangement for rapidly switching a load, in particular an inductive load, comprising:

- a switching transistor implemented as an N-channel MOS power transistor and connected as a high-side switch for connecting a load with a supply voltage,

- controllable switching means for applying a potential exceeding the voltage of the supply voltage source to the gate electrode of the switching transistor, wherein said switching means incorporate at least a first switching-means transistor whose collector current can flow at least in part to the gate electrode of the switching transistor during the ON state, and wherein the first switching-means transistor is connected as a current source.

2. The circuit arrangement according to Claim 1, wherein the first switching-means transistor connected as a current source is part of a current mirror circuit.

3. The circuit arrangement according to Claim 2, wherein the current mirror circuit additionally incorporates a first current mirror resistor and a second current mirror resistor each connected to a low voltage source on the one hand and the first current mirror resistor being connected to the base electrode and the current mirror resistor being connected to the emitter electrode of the first switching-means transistor on the other.

4. The circuit arrangement according to Claim 2, wherein the first switching-means transistor is a pnp transistor.

5. The circuit arrangement according to Claim 1, wherein the collector current of the first switching-means transistor flows to the gate electrode of the switching transistor via a diode connected in the flow direction.

6. The circuit arrangement according to Claim 2, wherein the ratio of the resistance values of the first current mirror resistor and the second current mirror resistor corresponds to approximately 100:1.

7. The circuit arrangement according to Claim 2, wherein an input current of the current mirror circuit is controllable by means of a second switching-means transistor connected as a current source and clocked by a control signals.

8. The circuit arrangement according to Claim 7, wherein the input current of the current mirror flows to the latter via an RC element comprising an RC element resistor and a parallel-connected RC element capacitor.

9. The circuit arrangement according to Claim 8, wherein the time constant of the RC element is so designed that the RC element-capacitor is not charged significantly during the turn-on time of the switching transistor, but virtually completely charged during its ON time.

10. The circuit arrangement according to Claim 2, wherein the current mirror circuit further includes a diode connected in series with the first current mirror resistor in and in the flow direction of the current mirror input current.

11. The circuit arrangement according to Claim 1, wherein a bootstrap capacitor is provided which is connected to the low voltage source on the one hand and to the source electrode of the switching transistor on the other.

12. The circuit arrangement according to Claim 3, wherein there is provided a bootstrap diode oriented in the forward direction for coupling the voltage of the low voltage source into the current mirror circuit.

13. The circuit arrangement according to Claim 3, wherein the low voltage source has an auxiliary voltage source sitting on top of the potential of the supply voltage.

14. The circuit arrangement according to Claim 1, wherein a third switching-means transistor is provided whose emitter electrode is connected to the gate electrode of the switching transistor and whose collector electrode is connected via a leakage resistor to the source electrode of the switching transistor.

15. The circuit arrangement according to Claim 14, wherein the base electrode of the third switching-means transistor is connected via a leakage resistor to the source electrode of the switching transistor.

16. The circuit arrangement according to Claim 14, wherein the third switching-means transistor is a pnp transistor.

17. The circuit arrangement according to Claim 5, wherein a third switching-means transistor is provided whose emitter electrode is connected to the gate electrode of the switching transistor and whose collector electrode is connected via a leakage resistor to the source electrode of the switching transistor, and wherein the diode via which the collector current of the first switching-means transistor flows to the gate electrode of the switching transistor is disposed between the collector of the first switching-means transistor and the emitter of the second switching-means transistor.

18. A method for rapidly switching a load, in particular an inductive load, comprising the steps of:

- connecting a load via a switching transistor implemented as an N-channel MOS power transistor with a supply voltage,

- applying a potential exceeding the voltage of the supply voltage source to the gate electrode of the switching transistor through switching means, wherein said switching means incorporate at least a first switching-means transistor whose collector current can flow at least in part to the gate electrode of the switching transistor during the ON state, and wherein the first switching-means transistor is connected as a current source.

19. The method according to Claim 18, wherein the collector current of the first switching-means transistor flows to the gate electrode of the switching transistor via a diode connected in the flow direction.

20. The method according to Claim 18, further comprising the step of providing a third switching-means transistor whose emitter electrode is connected to the gate electrode of the switching transistor and whose collector electrode is connected via a leakage resistor to the source electrode of the switching transistor.